PATENT ABSTRACTS OF JAPAN

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(71)Applicant : ANDO ELECTRIC CO LTD

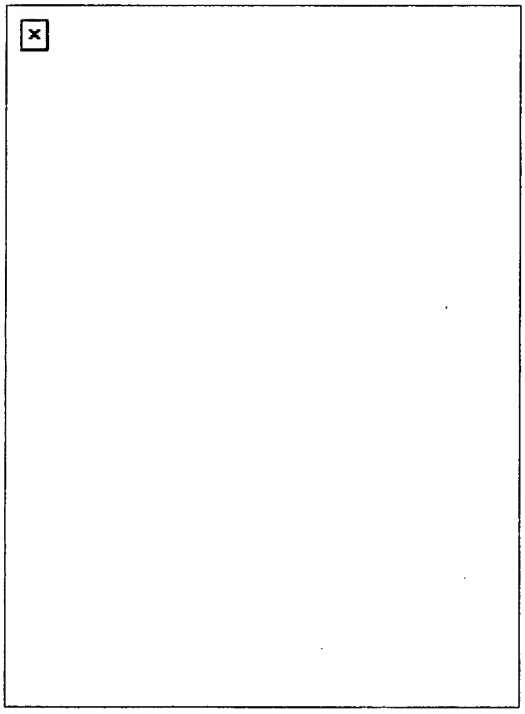
(72)Inventor : ODA TOSHIHIRO

(54) WAFER DEFECT ANALYZER

(57)Abstract:

PROBLEM TO BE SOLVED: To improve the efficiency of defect analysis by forming a fail bit map at the physical arrangement of a chip formed on a wafer from defect information by an operating part, selecting the chip displayed on the fail bit map, and forming the fail bit map at a memory-cell array unit.

SOLUTION: An operating part 30 reads wafer information Wi and chip information Ci1, Ci2... from a defect information file F stored in a memory part 20 and converts the information into the image data so that each chip is arranged at the specified position on the wafer. From pass/fail information DF1 of each memory-cell array and pass/fail information DF2 for every data bit or memory-cell array information D1, D2,..., color coding display is performed for the memory cell having the defect, and the display data are formed. Furthermore, the operating part 30 moves and displays a cursor C on a display part 40 and executes the function, which is assigned to a menu button 40b and the like for displaying the fail bit map at the memory-cell array unit of the specified chip.



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CLAIMS

[Claim(s)]
[Claim 1] The storage section which stores the defect information on the chip formed on the wafer, and the operation part which creates a fail bit map from said defect information by physical arrangement of said chip formed on said wafer, It has the display which displays said fail bit map, and the input section which outputs the actuation information according to actuation of an operator. Said operation part is wafer failure-analysis equipment characterized by choosing the chip displayed on said fail bit map according to the actuation information outputted from said input section, and creating the fail bit map of this chip per memory cell array.
[Claim 2] Said operation part is wafer failure-analysis equipment according to claim 1 characterized by creating the map in which the pass/fail for every data bit are shown from said defect information.
[Claim 3] Said operation part is wafer failure-analysis equipment according to claim 1 characterized by creating the map in which the pass/fail of the memory cell array unit of each chip are shown from said defect information.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the wafer failure-analysis equipment which analyzes the cause of a defect of the chip formed on the semi-conductor wafer.
[0002]
[Description of the Prior Art] The equipment which examines semiconductor memories, such as RAM (Random Access Memory), and analyzes a defect conventionally is invented. The above-mentioned semiconductor memory has many memory cells, and the address is assigned to each memory cell. In examining this semiconductor memory, it judges whether the memory cell to which the above-mentioned address was assigned is poor by specifying the address of a memory cell, writing a test data in the memory cell to which that address was assigned, beginning to read this written-in test data again, and comparing with a test data.
[0003] The fail bit map of a semiconductor memory is created by repeating the above-mentioned actuation and performing it, changing the address. When the above-mentioned semiconductor memory consists of one chip, the fail bit map of the chip will be obtained. And the gestalt of the defect generated by displaying the obtained fail bit map on a display etc. is analyzed.
[0004]
[Problem(s) to be Solved by the Invention] By the way, with conventional equipment, since a fail bit map was not able to obtain the display of distribution of the defect bit to all the chips formed on the semi-conductor wafer to one chip formed on the semi-conductor wafer, it had the problem that it was difficult to search for the inclination of defect bit generating distribution of the whole semi-conductor wafer.
[0005] This invention is made in view of the above-mentioned situation, and it aims at offering the wafer failure-analysis equipment which can perform analysis for each chip per memory cell array while it can analyze the inclination of defect generating distribution of the chip formed in the semi-conductor wafer.
[0006]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, invention according to claim 1 The storage section which stores the defect information on the chip formed on the wafer, and the operation part which creates a fail bit map from said defect information by physical arrangement of said chip formed on said wafer, It has the display which displays said fail bit map, and the input section which outputs the actuation information according to actuation of an operator. It is characterized by for said operation part choosing the chip displayed on said fail bit map according to the actuation information outputted from said input section, and creating the fail bit map of this chip per memory cell array. Invention according to claim 2 is characterized by said operation part creating the map in which the pass/fail for every data bit are shown from said defect information in wafer failure-analysis

equipment according to claim 1. Invention according to claim 3 is characterized by said operation part creating the map in which the pass/fail of the memory cell array unit of each chip are shown from said defect information in wafer failure-analysis equipment according to claim 1.

[0007]

[Embodiment of the Invention] Hereafter, 1 operation gestalt of this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing the outline configuration of the wafer failure-analysis equipment by 1 operation gestalt of this invention. If the wafer failure-analysis equipment by this operation gestalt is divided roughly as shown in drawing 1 As opposed to the defect information I memorized by the storage section 20 which memorizes the input section 10 for inputting directions of an operator, the defect information I on each chip formed on the wafer, etc., and the storage section 20 It consists of operation part 30 which performs the operation according to the directions of an operator inputted from the input section 10, and a display 40 which displays the result of an operation of operation part 30.

[0008] The above-mentioned input section 10 is a mouse, and when migration actuation is performed by the operator, it outputs the actuation signal according to the control input to operation part 30. Moreover, this input section 10 is equipped with carbon button 10a, and when pushed by the operator, it outputs a depression signal (the above-mentioned actuation signal and a depression signal make actuation information).

[0009] Although the storage section 20 is omitting illustration, since it stores the various information acquired from IC (Integrated Circuit) testing device, it is prepared. The above-mentioned defect information I is memorized by file format as a defect information file F. This defect information file F stores the chip information Ci1 and Ci2 about chips, such as a location to the above-mentioned normal coordinate of the chip formed on the semi-conductor wafer information Wi about wafers, such as the maximum number of X shaft orientations of the chip currently formed, and the number of the maximum numbers of Y shaft orientations, and a semi-conductor wafer, magnitude, and a test result, and --.

[0010] In addition, in case the above-mentioned X-axis and a Y-axis acquire various information from IC testing device, they are an orthogonal axis set up beforehand, and the zero is set up as the above-mentioned normal coordinate. Usually, the chip is formed in the shape of a matrix on the semi-conductor wafer, and each above-mentioned shaft is set up so that it may become the chip and parallel which were formed in the shape of a matrix on the semi-conductor wafer. The above-mentioned chip information Ci1 and Ci2 and -- are stored in condition, such as the information about the chip formed in the 0th line 0th train, information about the chip formed in the 0th line 1st train, ..., information about the chip formed in the 1st line 0th train, information about the chip formed in the 1st line 1st train, and .. In this case, the X-axis is set up in a train and this direction, and a Y-axis is set up in a line and this direction.

[0011] Moreover, the memory cell formed in the above-mentioned chip does not have independent each. It is constituted as a memory cell array formed in the shape of [which made plurality the unit] a matrix. The above-mentioned chip information Ci1 and Ci2 and -- It consists of pass/fail information DF 1 on each memory cell array, pass/fail information DF 2 for every data bit, memory cell array information D1 and D2, such as a location of each memory cell array, magnitude, the number of the maximum memory cell arrays of X shaft orientations, and the number of the maximum memory cell arrays of Y shaft orientations, and --. 22 is a memory buffer and memorizes the indicative data which is created based on the various information read from the defect information file F, and is displayed on a display 40, various registers, etc.

[0012] Operation part 30 reads the wafer information Wi and the chip information Ci1 and Ci2, and -- from the defect information file F memorized by the storage section 20. While the physical relationship of each chip and a wafer is calculated from each positional information

and each chip changes into image data on a wafer by which predetermined ****** is carried out From the chip information Ci1 and Ci2, pass/fail information DF 1 on each memory cell array contained in --, pass/fail information DF 2 for every data bit or the memory cell array information D1 and D2, and --, a classification-by-color display is performed to a memory cell with a defect, and an indicative data is created.

[0013] Moreover, operation part 30 displays Cursor C on a display 40, and indicates this cursor C by migration based on the actuation signal outputted from the input section 10. Moreover, when a depression signal is outputted from the input section 10, the function currently assigned to the menu buttons 40a-40d currently displayed on the location where Cursor C was displayed is performed, or it has the function which chooses one chip from two or more displayed chips. This operation part 30 is realized by ROM (Read OnlyMemory) which stored CPU (central processing unit) and various control programs.

[0014] The above-mentioned menu button 40a-40d of each displayed on a display 40 is menu button 40d for displaying menu button 40c for displaying menu button 40b for displaying the fail bit map in the memory cell array unit of menu button 40a for displaying the fail bit map of a wafer scale, and a specific chip, and the pass/fail for every bit, and the pass/fail of a memory cell array. Operation part 30 makes a display 40 display these menu buttons 40a-40d on the power up of wafer failure-analysis equipment.

[0015] Next, actuation of the wafer failure-analysis equipment by 1 operation gestalt of this invention is explained.

(1) The indicator chart 2 of the fail bit map of a wafer scale is a flow chart which shows the actuation in the case of displaying the fail bit map of a wafer scale. An operator does migration actuation of the input section 10, and moves Cursor C to the location where menu button 40a is displayed. If an operator does the depression of the carbon button 10a with which the input section 10 was equipped in this condition, a depression signal will be outputted to operation part 30 from the input section 10. If this depression signal is inputted, operation part 30 will read the defect information file F stored in the storage section 20 (step SA 1).

[0016] Next, operation part 30 creates two registers which make the contents of a count memorize in a memory buffer 22, and initializes the contents to "0" while it stores information, such as the maximum number of the chip of the wafer information Wi stored in the read defect information file F, and X shaft orientations, and the maximum number of the chip of Y shaft orientations, in a memory buffer 22 (step SA 2).

[0017] At a step SA 3, the contents [on the other hand / (Y register is called hereafter)] of the above-mentioned register are compared with the maximum number of the chip of Y shaft orientations, and it is judged whether the contents of the Y register are more than the maximum number of the chip of Y shaft orientations. When this decision result is "NO", it progresses to a step SA 4. At a step SA 4, the contents of another side (X register is called hereafter) of the above-mentioned register are compared with the maximum number of the chip of X shaft orientations, and it is judged whether the contents of the X register are more than the maximum number of the chip of X shaft orientations. When this decision result is "NO", it progresses to a step SA 5.

[0018] At a step SA 5, the chip information Ci1 and Ci2 and one chip information in -- are read based on the contents of X register and the Y register. For example, since the contents of the X register and the contents of the Y register are "0" at first [both], the chip information about the chip arranged on the 0th line 0th train is read. Next, processing which creates an indicative data based on the wafer information stored in buffer memory 22 at this chip information and step SA 1 is performed. This indicative data consists of a frame of a chip, and based on the chip information on the above-mentioned chip, when that chip is faulty, within the limit [of that chip] is smeared away in red. At this time, the frame of the above-mentioned chip is actually arranged on the location corresponding to the location where that chip is formed on the wafer.

After the above processing is completed, operation part 30 increments the contents of the X register, and returns to a step SA 4.
[0019] On the other hand, when the decision result of a step SA 4 is "YES", operation part 30 increments the contents of the Y register, and returns to a step SA 3. That is, in processing from a step SA 3 to a step SA 5, the indicative data which shows poor distribution is created to all the chips formed on the wafer. The created indicative data is stored in buffer memory 22.
[0020] When the decision result in a step SA 3 is "YES", processing progresses to a step SA 6, and the indicative data stored in the memory buffer 22 is read by operation part 30, it is outputted to a display 40, and the fail bit map of a wafer scale as shown in drawing 1 is displayed.
[0021] This fail bit map is shown in drawing 3 (a), drawing 3 (b), drawing 4 (a), and drawing 4 (b). Drawing 3 and drawing 4 are drawings showing the example of the fail bit map of a wafer scale. In these drawings, the part smeared away is a fault. Drawing 3 (a) is the example of the fail bit map displayed when a defect common between each chip arises, and drawing 3 (b) is the example of a fail bit map when common [between shots / poor] arises. Moreover, drawing 4 (a) is the example of a fail bit map when a defect arises in the specific region of a wafer, and drawing 4 R> 4 (b) is a fail bit map when the poor circumference of a wafer is generated.
[0022] The time amount required in order that the defect class of chip formed in the wafer by displaying the fail bit map of a wafer scale as shown in drawing 3 and drawing 4 can identify at a glance and may find out the cause of a defect, as explained above can be shortened. Moreover, it can judge which process of chip creation time should be improved by taking statistics of occurrence frequency according to defect's class.
[0023] (2) The indicator chart 5 of the map in the memory cell array unit of a specific chip is a flow chart which shows the actuation in the case of displaying the map in the memory cell array unit of a specific chip. If an operator does migration actuation of the input section 10, and arranges Cursor C in the location of a specific chip and the depression of the carbon button 10a is carried out in the condition that the fail bit map of a wafer scale is displayed as shown in drawing 1 R> 1, a depression signal will be outputted from the input section 10.
[0024] If this depression signal is inputted, operation part 30 will indicate the chip currently displayed on the display position of Cursor C, for example by blue, and will emphasize the purport as which that chip was chosen (step SB 1). Next, an operator does migration actuation of the input section 10, and moves Cursor C to the location where menu button 40b was displayed. And if an operator does the depression of the carbon button 10a, a depression signal will be outputted from the input section 10 (step SB 2).
[0025] If the above-mentioned depression signal is inputted, operation part 30 reads the chip information on the chip chosen at a step SB 1 from the defect information file F, and stores the number of the maximum memory cell arrays of X shaft orientations of this chip information, and the number of the maximum memory cell arrays of Y shaft orientations in a memory buffer 22. Moreover, operation part 30 creates two registers which make the contents of a count memorize in a memory buffer 22, and initializes the contents to "0" (step SB 3).
[0026] At a step SB 4, the contents [on the other hand / (Y register is called hereafter)] of the above-mentioned register are compared with the number of the maximum memory cell arrays of Y shaft orientations, and it is judged whether the contents of the Y register are more than the number of the maximum memory cell arrays of Y shaft orientations. When this decision result is "NO", it progresses to a step SB 5. At a step SB 5, the contents of another side (X register is called hereafter) of the above-mentioned register are compared with the number of the maximum memory cell arrays of X shaft orientations, and it is judged whether the contents of the X register are more than the maximum number of the chip of X shaft orientations. When this decision result is "NO", it progresses to a step SB 6.
[0027] At a step SB 6, the memory cell array information D1 and D2 and -- are read from the

chip information read in a step SB 3 based on the contents of X register and the Y register. Since the contents of the X register and the contents of the Y register are "0" at first [both], the memory cell array information about the memory cell array allotted to the 0th line 0th train is read. Next, processing which creates an indicative data is performed based on this memory cell array information. This indicative data consists of a frame of a chip, and a frame of the memory cell in a chip, and based on the memory cell information on each memory cell, when that memory cell is poor, within the limit [of that memory cell] is smeared away in red. At this time, the frame of the above-mentioned memory cell is actually arranged on the location corresponding to the location where that memory cell is actually formed in the chip. After the above processing is completed, operation part 30 increments the contents of the X register, and returns to a step SB 5.

[0028] On the other hand, when the decision result of a step SB 5 is "YES", operation part 30 increments the contents of the Y register, and returns to a step SB 4. That is, in processing from a step SB 4 to a step SB 6, to all the memory cells in a chip, it is poor or the indicative data which shows distribution of no is created. The created indicative data is stored in buffer memory 22.

[0029] When the decision result in a step SB 4 is "YES", processing progresses to a step SB 7, and the indicative data stored in the memory buffer 22 is read by operation part 30, it is outputted to a display 40, and the map in the memory cell array unit of a specific chip as shown in drawing 6 is displayed. The part in which it was smeared away in drawing 6 is a fault.

[0030] As explained above, when the fail bit map of a wafer scale as shown in drawing 3 (a) is displayed and the cause of a defect of a certain specific circuit is presumed Since a specific chip is expanded and the map in a memory cell array unit was displayed Since the defect of circumference circuits, such as a decoder and a sense-amplifier circuit, related to the memory cell array in which a defect bit exists is easily discoverable, the effectiveness of failure analysis can improve and it can contribute to improvement in a step stop.

[0031] (3) The indicator chart 7 of the pass/fail for every data bit is a flow chart which shows the actuation in the case of displaying the pass/fail for every data bit. First, an operator does migration actuation of the input section 10, and moves Cursor C to the location where menu button 40c is displayed. If an operator does the depression of the carbon button 10a with which the input section 10 was equipped in this condition, a depression signal will be outputted to operation part 30 from the input section 10 (step SC 1).

[0032] If this depression signal is inputted, operation part 30 will create two registers which make the contents of a count memorize in a memory buffer 22, and will initialize those contents to "0" while it acquires information, such as a location of the wafer information Wi stored in the memory buffer 22, i.e., a wafer, a path of a wafer, the maximum number of the chip of X shaft orientations, and the maximum number of the chip of Y shaft orientations, (step SC 2). In addition, the above-mentioned wafer information Wi is stored in the memory buffer 22 by processing of the step SA 2 in drawing 2 in the case of displaying the fail bit map of (1) wafer scale mentioned above.

[0033] At a step SC 3, the contents [on the other hand / (Y register is called hereafter)] of the above-mentioned register are compared with the maximum number of the chip of Y shaft orientations, and it is judged whether the contents of the Y register are more than the maximum number of the chip of Y shaft orientations. When this decision result is "NO", it progresses to a step SC 4. At a step SC 4, the contents of another side (X register is called hereafter) of the above-mentioned register are compared with the maximum number of the chip of X shaft orientations, and it is judged whether the contents of the X register are more than the maximum number of the chip of X shaft orientations. When this decision result is "NO", it progresses to a step SC 5.

[0034] At a step SC 5, the chip information Ci1 and Ci2 and one chip information in -- are read based on the contents of X register and the Y register. For example, since the contents of the X register and the contents of the Y register are "0" at first [both], the chip information about the chip arranged on the 0th line 0th train is read. Next, an indicative data is created based on this chip information, the wafer information acquired from buffer memory 22 at a step SC 2, and pass/fail information DF 2 for every data bit. This indicative data consists of a frame of a wafer, and a frame of each chip formed in the wafer, and based on pass/fail information DF 2 for every above-mentioned data bit, when that data bit is poor, within the limit [of that chip] is smeared away in red. After the above processing is completed, operation part 30 increments the contents of the X register, and returns to a step SC 4.
[0035] On the other hand, when the decision result of a step SC 4 is "YES", operation part 30 increments the contents of the Y register, and returns to a step SC 3. That is, in processing from a step SC 3 to a step SC 5, the indicative data of the distribution which shows distribution with a poor data bit is created to all the chips formed on the wafer. The created indicative data is stored in buffer memory 22.
[0036] When the decision result in a step SC 3 is "YES", processing progresses to a step SC 6, and the indicative data stored in the memory buffer 22 is read by operation part 30, it is outputted to a display 40, and the pass/fail of the data bit for every data bit of a wafer scale as shown in drawing 8 are displayed. Drawing 8 is the map which expressed drawing 4 (b) with pass/fail display for every data bit. In this drawing, the pass/fail of the data bit of a chip which has four data bits are shown, and the part of a fail has become the smeared-away display.
[0037] From the map of a chip with arrangement of complicated data bits when some data bits are intermingled in a memory cell array, in case a data bit is arranged irregularly, the pass/fail of a data bit are not known easily. For example, when it succeeds in the display shown in drawing 4 (b) when the chip which has four data bits like drawing 9 was arranged on eight memory cell arrays, it is difficult to recognize the pass/fail of a data bit easily. When still more complicated, it is still more so. The above-mentioned map can know easily the data bit which became a defect on a scale of the wafer irrespective of arrangement of a data bit by displaying the pass/fail of a data bit.
[0038] (4) The indicator chart 10 of the pass/fail of a memory cell array is a flow chart which shows the actuation in the case of displaying the pass/fail of a memory cell array. First, an operator does migration actuation of the input section 10, and moves Cursor C to the location where menu button 40d is displayed. If an operator does the depression of the carbon button 10a with which the input section 10 was equipped in this condition, a depression signal will be outputted to operation part 30 from the input section 10 (step SD 1).
[0039] If this depression signal is inputted, operation part 30 will create two registers which make the contents of a count memorize in a memory buffer 22, and will initialize those contents to "0" while it acquires information, such as a location of the wafer information Wi stored in the memory buffer 22, i.e., a wafer, a path of a wafer, the maximum number of the chip of X shaft orientations, and the maximum number of the chip of Y shaft orientations, (step SD 2). In addition, the above-mentioned wafer information Wi is stored in the memory buffer 22 by processing of the step SA 2 in drawing 2 in the case of displaying the fail bit map of (1) wafer scale mentioned above.
[0040] At a step SD 3, the contents [on the other hand / (Y register is called hereafter)] of the above-mentioned register are compared with the maximum number of the chip of Y shaft orientations, and it is judged whether the contents of the Y register are more than the maximum number of the chip of Y shaft orientations. When this decision result is "NO", it progresses to a step SD 4. At a step SD 4, the contents of another side (X register is called hereafter) of the above-mentioned register are compared with the maximum number of the chip of X shaft orientations, and it is judged whether the contents of the X register are more

than the maximum number of the chip of X shaft orientations. When this decision result is "NO", it progresses to a step SD 5.
[0041] At a step SD 5, the chip information Ci1 and Ci2 and one chip information in -- are read based on the contents of X register and the Y register. For example, since the contents of the X register and the contents of the Y register are "0" at first [both], the chip information about the chip arranged on the 0th line 0th train is read. Next, based on the wafer information acquired from buffer memory 22, and pass/fail information DF 1 on a memory cell array, an indicative data is created at this chip information and step SD 2. This indicative data consists of the frame of a wafer, a frame of each chip formed in the wafer, and a frame of the above-mentioned memory cell array, and based on pass/fail information DF 1 on each above-mentioned memory cell array, when that chip is faulty, within the limit [of that memory cell array] is smeared away in red. After the above processing is completed, operation part 30 increments the contents of the X register, and returns to a step SD 4.
[0042] On the other hand, when the decision result of a step SD 4 is "YES", operation part 30 increments the contents of the Y register, and returns to a step SD 3. That is, in processing from a step SD 3 to a step SD 5, the indicative data which shows distribution with a poor memory cell array is created to all the chips formed on the wafer. The created indicative data is stored in buffer memory 22.
[0043] When the decision result in a step SD 3 is "YES", processing progresses to a step SD 6, and the indicative data stored in the memory buffer 22 is read by operation part 30, it is outputted to a display 40, and the pass/fail of the memory cell array of a wafer scale as shown in drawing 11 are displayed. Drawing 11 is the map which displayed the fail bit map of drawing 4 (b) by the pass/fail of a memory cell array. The display by which the part with the fail of the memory cell array formed in the chip was smeared away is made.
[0044] Thus, since the pass/fail of a memory cell array are displayed on a scale of a wafer, it can distinguish common [of the memory cell array during a chip / poor].
[0045]
[Effect of the Invention] Since the fail bit map of all the chips created on the wafer is displayed according to invention according to claim 1 as explained above, the time amount required in order that the defect class of chip formed in the wafer can identify at a glance and may find out the cause of a defect can be shortened. Moreover, since a specific chip is expanded, the fail bit map in a memory cell array unit is displayed and the defect of circumference circuits, such as a decoder and a sense-amplifier circuit, related to the memory cell array in which a defect bit exists is easily discoverable, the effectiveness of failure analysis can improve and it can contribute to improvement in a step stop. According to invention according to claim 2, since the pass/fail of a data bit are displayed on a scale of a wafer, the fault of a data bit can be known easily. Moreover, even if it is the chip which has a complicated data bit, the condition of a data bit can be known easily. According to invention according to claim 3, since the pass/fail of a memory cell array are displayed on a scale of a wafer, it can distinguish common [of the memory cell array during a chip / poor].

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the outline configuration of the wafer failure-analysis equipment by 1 operation gestalt of this invention.
[Drawing 2] It is the flow chart which shows the actuation in the case of displaying the fail bit map of a wafer scale.
[Drawing 3] It is drawing showing the example of the fail bit map of a wafer scale.
[Drawing 4] It is drawing showing the example of the fail bit map of a wafer scale.
[Drawing 5] It is the flow chart which shows the actuation in the case of displaying the fail bit map in the memory cell array unit of a specific chip.
[Drawing 6] It is drawing showing the example of the map in the memory cell array unit of a specific chip.
[Drawing 7] It is the flow chart which shows the actuation in the case of displaying the pass/fail for every data bit.
[Drawing 8] It is the map which displayed the pass/fail for every data bit on a scale of the wafer.
[Drawing 9] Arrangement of a data bit is drawing showing the partition of the data bit of a complicated chip.
[Drawing 10] It is the flow chart which shows the actuation in the case of displaying the pass/fail of a memory cell array.
[Drawing 11] It is the map which displayed the pass/fail of a memory cell array on a scale of the wafer.
[Description of Notations]
10 Input Section
20 Storage Section
30 Operation Part
40 Display

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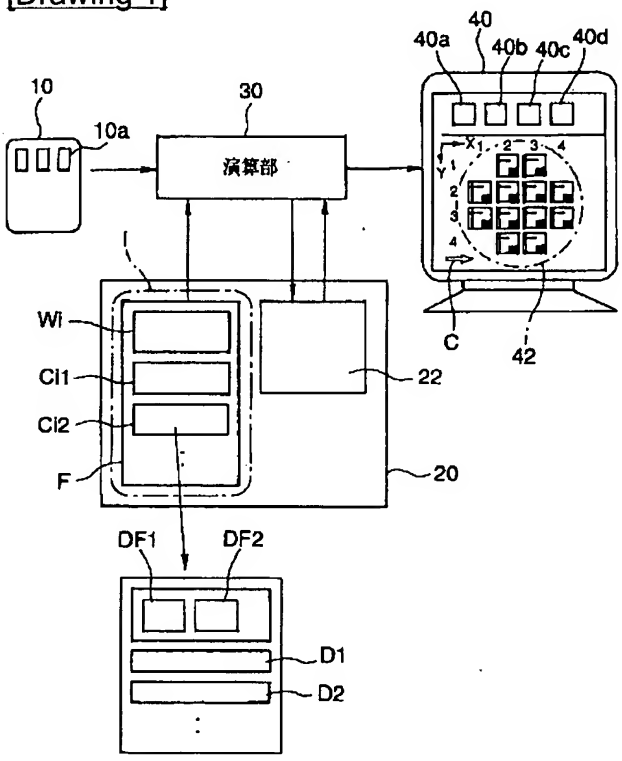
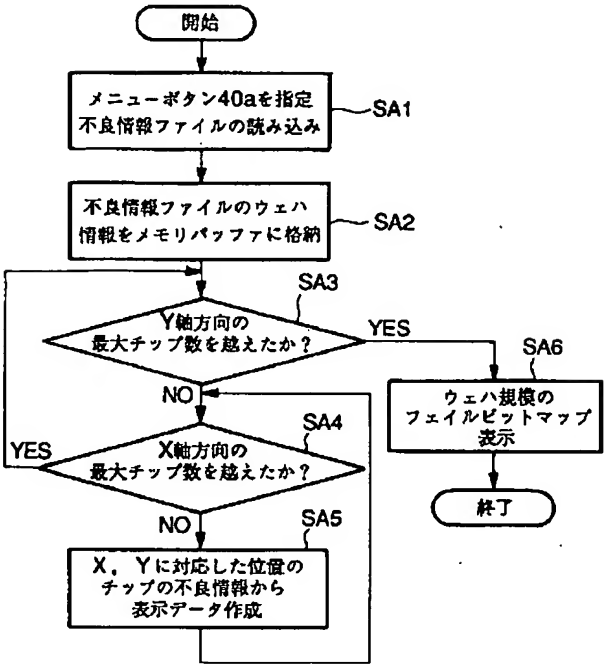
DRAWINGS

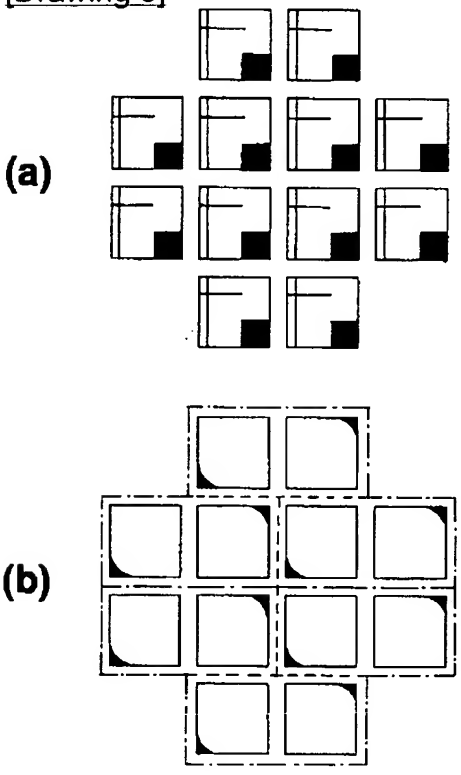
[Drawing 1]



[Drawing 2]

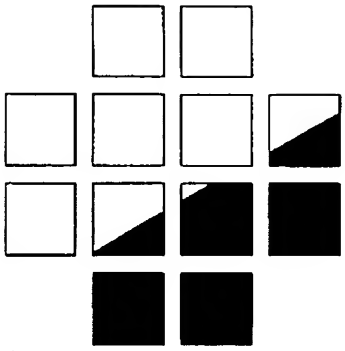


[Drawing 3]

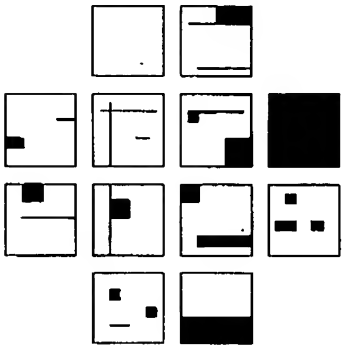


[Drawing 4]

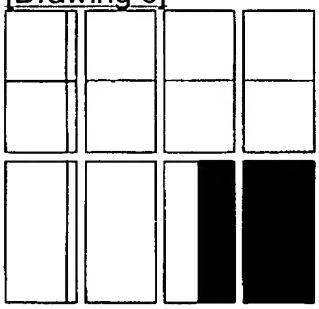
(a)



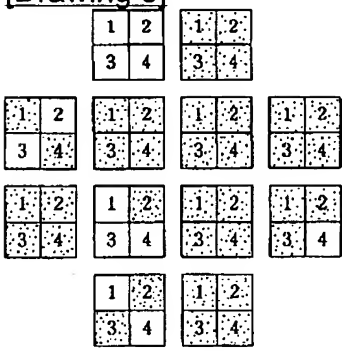
(b)



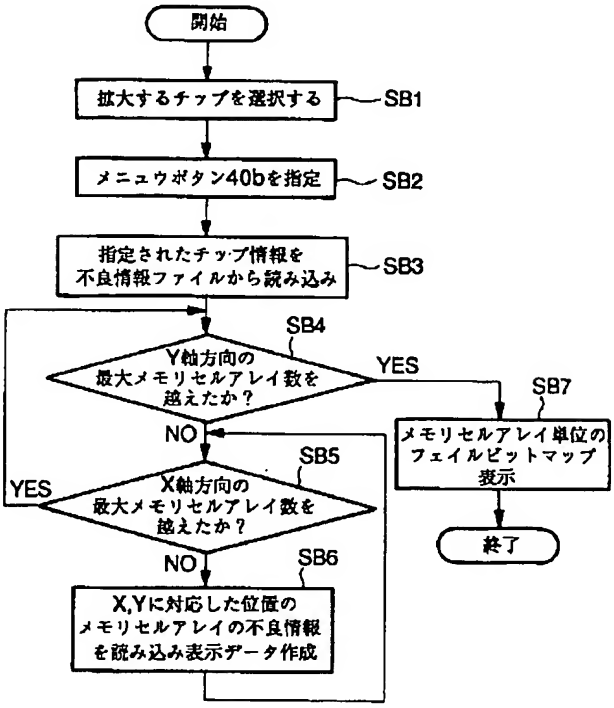
[Drawing 6]



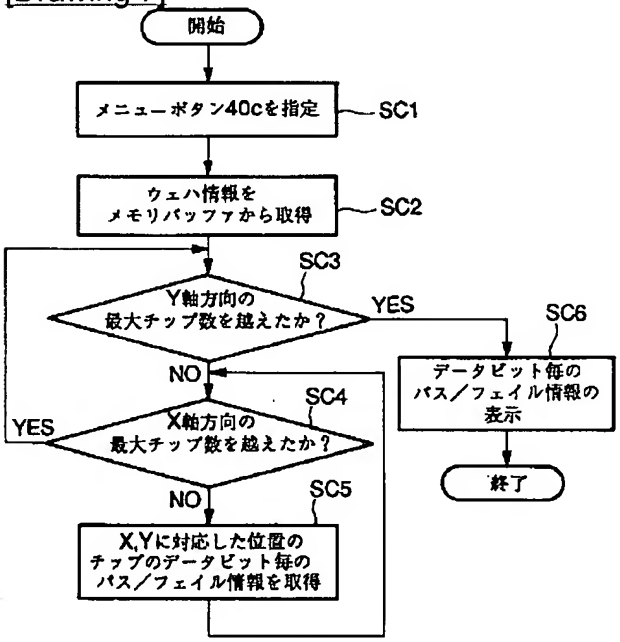
[Drawing 8]



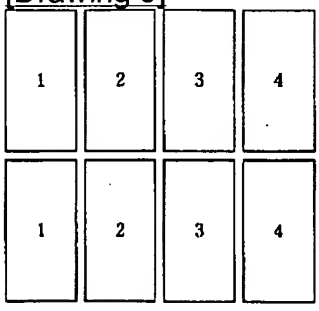
[Drawing 5]



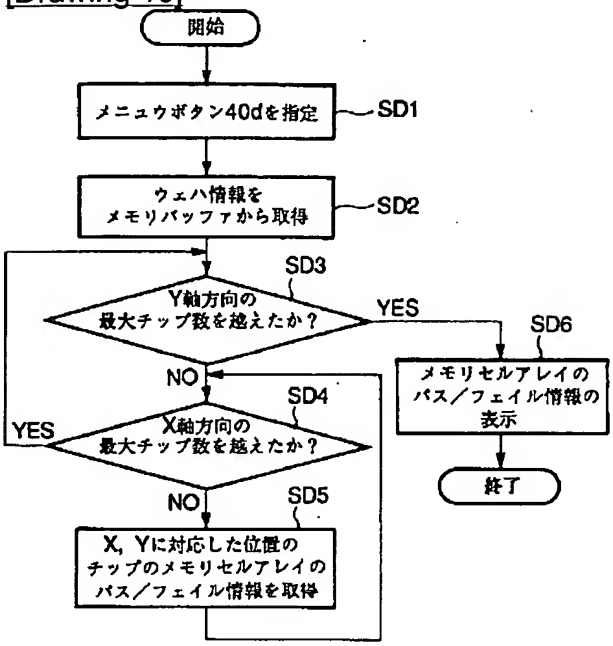
[Drawing 7]



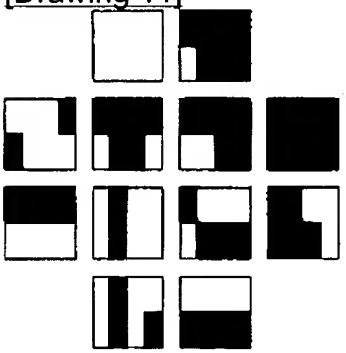
[Drawing 9]



[Drawing 10]



[Drawing 11]



[Translation done.]